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Low-Voltage Photovoltaic System Based on a Continuous Input/Output Current Converter

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Abstract: Low-voltage photovoltaic systems are being widely used around the world, including their introduction into the power grid. The development of these systems requires the adaptation of several power converters, their static and dynamic modeling, the design of passive elements, and the design of the controller parameters, among other actions. Today, power converters are key elements in the development of photovoltaic systems, and classical power converters such as buck converters produce discontinuous input and output currents, requiring a high input capacitance and impacting the output power quality of these systems. This paper presents a proposal for a low-voltage photovoltaic system that uses a continuous input/output current buck converter, which enhances the operation of the classical buck converter in photovoltaic systems. The methodology describes the proposed photovoltaic system, including the power converter, its detailed operation, and the analysis of its waveforms. Moreover, the methodology includes a mathematical model of the photovoltaic system's dynamic behavior and the design of a sliding-mode controller for maximum power extraction and perturbation rejection. The photovoltaic system is validated in two ways: first, a comparison with the classical buck converter highlighting the advantages of continuous input/output currents is presented; then, an application example using commercial devices is described in detail. The application example uses a flowchart to design the power converter and the sliding-mode controller, and a circuit simulation confirms the advantages of the continuous input/output current buck converter with its controller. In the circuit simulation, the control strategy is formed by a perturb and observe algorithm that generates the voltage reference for the sliding-mode controller, which guarantees the system stability, tracks the maximum power point, and rejects the double-frequency oscillations generated by an intended microinverter.

Keywords: continuous current; improved reliability; microinverter; non-electrolytic capacitor; power converter; sliding-mode controller; buck converter

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1. Introduction

Photovoltaic (PV) systems continue to be established as one of the most important renewable energy sources all around the world, since the installed capacity grows year after year. In 2021, about 175 GW were installed and commissioned, reaching a global installed capacity of 942 GW [1]. Moreover, according to the IEA, the Net Zero Emissions by 2050 scenario requires a significant increment in annual PV generation in the next years [2], which suggests that PV systems will continue growing in the future.

Typically, a grid-connected PV system is formed by a PV array, a capacitor (C_{pv}), a dc/dc converter, a dc-link capacitor, a dc/ac converter, and a control system [3]. The PV array transforms the light power into electric power and is connected to the dc/dc converter through C_{pv}, while the dc/dc converter modifies the array operating voltage to extract the maximum power from the array. Moreover, the dc/dc converter delivers its power to a dc-link capacitor (or a battery [4,5]), which forms a dc bus used by the dc/ac converter, whose main function is to deliver the power to ac loads, the grid, or both. The control

system has three main objectives: The first one is to extract the maximum power from the PV array by using a maximum power point tracking (MPPT) technique, which generates a reference for the PV array voltage (or current). The second objective is to track the voltage (or current) reference generated by the MPPT with a controller to reject disturbances that may produce oscillations in the PV power or malfunction of the MPPT algorithm. The third objective of the control system is to inject the PV power to the grid, which requires synchronization with the grid voltage and injecting ac current to keep the dc-link capacitor voltage approximately constant [3].

Step-up dc/dc converters are widely used in grid-connected PV systems since the dc-link voltage is usually greater than the PV array voltage (hundreds of volts [6,7]). However, there are commercial inverters to supply ac loads where the dc-link voltage may be between 12 V and 70 V, such as off-grid PV inverters (e.g., [8–11]), PV inverters that can operate on-grid or off-grid (e.g., hybrid PV inverters [12–14]), and inverters supplied by a dc bus or a battery (e.g., [15–18]). In these applications, the inverter's nominal input voltage corresponds to the battery's nominal voltage (between 12 V and 70 V), while the PV array voltage is greater than those values due to the typical connection of PV modules in series and parallel to form the array. Therefore, step-down converters are required to couple the PV array to the dc bus.

In the literature, the buck converter is the most widely used step-down topology for PV systems to extract the maximum power from the PV generator, due to its simplicity, low number of components, and simple controllers [19]. However, the buck converter may be used in different forms depending on the PV system's structure to couple the PV array to a dc bus [4,20], charge a battery that feeds a stand-alone inverter [4], feed a boost converter that elevates the voltage for a grid-connected inverter [20], regulate the dc bus voltage [21] or current [22,23] that feeds an inverter, and implement multilevel inverters [5,24], among others.

There are also different MPPT strategies in the PV systems discussed before. Although the two main implemented MPPT algorithms are perturb and observe (P&O) [4,5,22] and Incremental Conductance (IC) [20,23,24], some authors do not include an MPPT technique in the control system [21]. Moreover, some MPPT techniques generate the duty cycle of the buck converter with P&O [4,5] or IC [20,24] algorithms, while, in other systems, the output of the MPPT techniques is a reference of the PV array voltage [22] or current [23] with P&O or IC algorithms, respectively. At this point, it is important to mention that the MPPT algorithms that generate the converter's duty cycle are simpler to implement, but they cannot reject disturbances in the PV array voltage or current, which may produce unexpected variations in the power harvested from the PV array and, in some cases, the malfunction of the MPPT [25]. In a PV array connected to an inverter, one of the main perturbations is the 100 Hz or 120 Hz oscillations in the PV array voltage produced by the 50 Hz or 60 Hz ac voltage generated by the inverter [25]. That is why it is common to implement compensators for the PV array voltage or current in the dc/dc converter connected to the array.

Moreover, most of the discussed PV systems use linear compensators [22,26], while others propose more complex alternatives [27,28]. Linear compensators are implemented to track a voltage [22] or current [23] reference generated by the MPPT technique; nevertheless, although the linear compensators described before can reject perturbations in the PV array voltage [22] or current [23], only the compensator proposed in [22] rejects the 100 Hz or 120 Hz oscillations in the PV array voltage produced by the inverter. Regarding the more complex controllers, it is possible to find a deadbeat controller of the PV array current that generates the converter's duty cycle with an explicit expression, which can be easily implemented on a microcontroller [27]. Moreover, in [28], the authors use a cascade controller, where the inner loop is a sliding-mode controller of the inductor current and the outer loop is a P controller that tracks the PV array voltage reference generated by the MPPT technique.

In the PV systems described before, it is important to highlight that the input current of the buck converter connected to the PV arrays is discontinuous, since it corresponds to the MOSFET current [29]; therefore, it is necessary to use an input capacitor (C_{pv}) in the range of hundreds of μF (e.g., [21,23]) or even thousands of μF (e.g., [26,30]) to obtain a continuous current in the PV array. Such capacitance ranges can be obtained with electrolytic capacitors [31], which not only have a shorter lifetime than other capacitors and affect converter reliability [31,32], but also have increased cost and weight [33].

One feasible option to reduce the capacitance of C_{pv} and avoid the use of electrolytic capacitors is to replace the buck converter with the topology denominated, from here on, as a continuous input/output current (CIOC) buck converter (also known as super-buck converter), which is formed by two inductors, one capacitor, one MOSFET, and one diode [34,35]. This converter provides a continuous input current, which allows a significant reduction in the C_{pv} capacitance, with the same input–output voltage and current ratios of the buck converter [34,35]. Although the CICO buck converter was originally proposed for a rectifier with power factor correction [36], it has also been used for different applications, such as dc voltage regulation for resistive loads [37,38] or generic loads [39–41], as well as the battery interface for a dc bus [42,43]. Nevertheless, to the best knowledge of the authors, it has only been used to extract the power from a PV array in [44].

The PV system proposed in [44] is formed by a PV module, a CICO buck, a battery, and an output capacitor (between the converter's output and the battery). The paper proposes a cascade controller, where the inner loop tracks the PV array's current reference generated by an MPPT algorithm, and the outer loop regulates the output voltage; however, the outer loop is only active when the output voltage surpasses the maximum voltage defined for the system. The controllers proposed in [44] are based on the small-signal model of the system and include stability analysis; additionally, the paper includes experimental results with the controller implemented with analog circuits. However, the proposed PV system uses two additional capacitors regarding the basic CIOC buck topology (i.e., output capacitor and C_{pv}), and C_{pv} is in the range of electrolytic capacitors (C_{pv} = 1 mF), which reduces the converter reliability and increases its cost and weight. Additionally, the MPPT algorithm is not implemented, and the proposed PV array current controller is not clearly explained. Moreover, the paper does not include a procedure or guideline to design the PV array current controller, and it is not able to reject 100 Hz or 120 Hz oscillations in the PV array voltage if the proposed system is connected to an inverter.

Therefore, this paper proposes a PV system based on the CICO buck converter along with a control strategy and a design procedure for PV systems, where the array voltage is greater than the dc bus voltage and the power is delivered to the grid or ac loads. The adopted converter does not require an output capacitance, and the input capacitance is significantly lower than the one required by a PV system based on a buck converter; hence, it can be implemented with non-electrolytic capacitors. Furthermore, the proposed control strategy is inspired by the one proposed in [45], and it is formed by a P&O algorithm that generates the PV array voltage reference for a sliding-mode controller (SMC) that guarantees the system stability for any operating point and rejects the 100 or 120 Hz oscillations produced by the inverter. Finally, the paper also includes a design procedure of the proposed converter's inductors and capacitors and SMC's parameters considering the maximum voltage and current ripples, as well as the system's stability. The proposed system is evaluated for a realistic study case using a professional software simulation of power electronics and commercial devices as a reference. In summary, the main contributions of the paper are (1) a PV system based on the CIOC buck with an MPPT technique formed by a P&O algorithm that generates the reference of the PV array voltage and an SMC that tracks such a reference, (2) a detailed design procedure of the SMC's parameters to guarantee the system's stability for any operation, and (3) a design procedure of the converter's storage elements to guarantee the maximum ripples defined by the designer.

The rest of the paper is organized as follows: Section 2 describes the CIOC buck converter, Section 3 introduces the model of the proposed PV system that uses the CIOC

buck converter, Section 4 shows a comparison of a PV system based on buck converter and the proposed PV system, Section 5 presents the proposed SMC controller for MPPT, Section 6 contains the design procedure along with an application example, Section 7 introduces the circuital implementation and the simulation results, and finally, Section 8 presents the conclusions.

2. Continuous Input/Output Buck Converter for PV Applications

The proposed PV system based on the continuous input/output current (CIOC) buck converter is depicted in Figure 1. Such a PV system description includes the controller required to mitigate environmental and load perturbations, which is discussed in Section 5; the algorithm to track the maximum power point (MPPT), which in this case is the perturb and observe algorithm (P&O); and a filter needed to ensure global stability, which is discussed in Section 5.6. The load of the PV system is modeled using the voltage source v_o, which represents the input of an inverter. The PV source is connected at the CIOC buck converter, where the main advantage of the CIOC converter concerns the continuous input current requested to the PV source, which reduces the input capacitor C_{pv} in comparison with the classical buck converter; such an advantage is demonstrated in Section 4. In addition, the CIOC converter also provides a continuous current i_o to the load (inverter), thus providing a high power quality in comparison with converters with discontinuous output current.

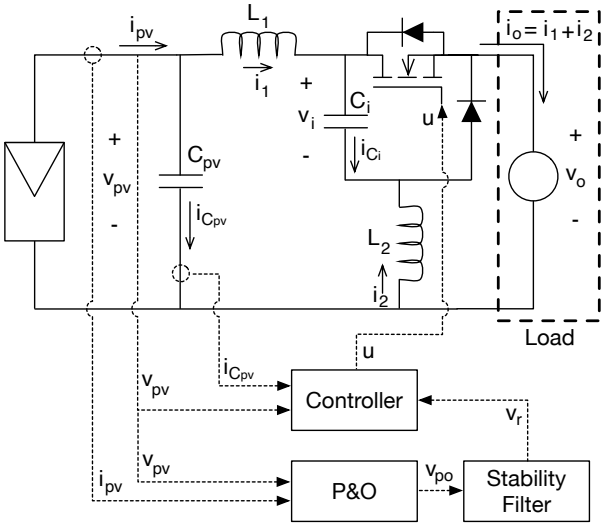

Figure 1. PV system based on the CIOC buck converter.

The CIOC buck converter is formed by a MOSFET and a diode, where the control signal u provided by the controller defines the state of those semiconductors. Moreover, the converter has two inductors (L_1 and L_2), an internal capacitor (C_i) and an input capacitor to regulate the PV source (C_{pv}). The P&O algorithm measures the PV current and voltage (i_{pv} and v_{pv}) to track the optimal PV voltage v_{po}, as it is described in [46,47]. Then, such an optimal value is processed by the stability filter to generate the controller reference v_r.

The following subsections describe the behavior of the PV system, based on the CIOC buck converter, in the two operation topologies generated by $u = 1$ and $u = 0$, i.e., when the MOSFET is closed and open, respectively.

2.1. Topology 1 ($u = 1$)

The fist topology occurs when the control signal is $u = 1$, which closes the MOSFET and opens the diode, which results in the equivalent circuit reported in Figure 2. The topology shows that the input current of the CIOC buck converter is equal to the current of the L_1 inductor, named i_1; hence, it is a continuous input current. In this topology, the internal capacitor C_i is discharged by the current of L_2 (i_2), thus providing additional power to the

load. Finally, the topology shows that the internal capacitor C_i provides a path connecting L_1 and L_2, while the MOSFET (closed) provides a path connecting both inductors with the load. Therefore, the output current i_o is equal to the sum of both L_1 and L_2 currents, which enables the CIOC buck converter to provide a continuous current to the load.

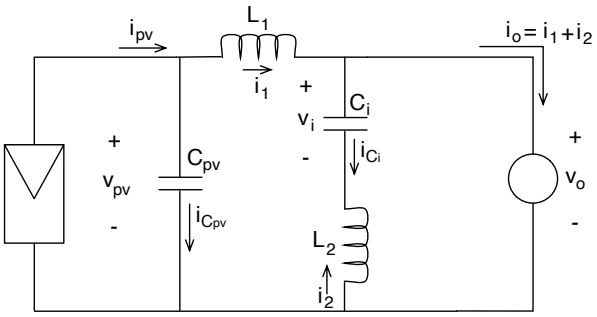

Figure 2. Topology 1 of the PV system based on the CIOC buck converter.

The differential equations modeling this topology are

$$\frac{di_1}{dt} = \frac{v_{pv} - v_o}{L_1} \tag{1}$$

$$\frac{di_2}{dt} = \frac{v_i - v_o}{L_2} \tag{2}$$

$$\frac{dv_i}{dt} = \frac{-i_2}{C_i} \tag{3}$$

$$\frac{dv_{pv}}{dt} = \frac{i_{pv} - i_1}{C_{pv}} \tag{4}$$

In addition, the MOSFET current (i_M) and diode voltage (v_D) are

$$i_M = i_o = i_1 + i_2 \tag{5}$$

$$v_D = -v_i \tag{6}$$

2.2. Topology 0 ($u = 0$)

The second topology occurs when the control signal is $u = 0$, which opens the MOSFET and closes the diode. The equivalent circuit is reported in Figure 3, which also shows that the input current of the CIOC buck converter is i_1. In this topology, the internal capacitor C_i is charged by the current of L_1 (i_1), and it also provides the path connecting L_1 and L_2, while the diode (closed) provides a path connecting both inductors with the load. Therefore, as in the previous topology, the output current i_o is continuous and equal to the sum of both i_1 and i_2.

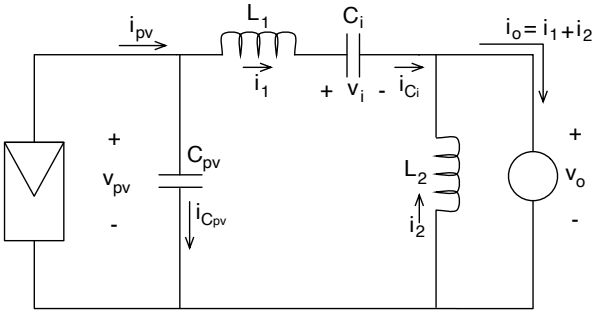

Figure 3. Topology 0 of the PV system based on the CIOC buck converter.

The differential equations modeling this topology are

$$\frac{di_1}{dt} = \frac{v_{pv} - v_o - v_i}{L_1} \tag{7}$$

$$\frac{di_2}{dt} = \frac{-v_o}{L_2} \tag{8}$$

$$\frac{dv_i}{dt} = \frac{i_1}{C_i} \tag{9}$$

$$\frac{dv_{pv}}{dt} = \frac{i_{pv} - i_1}{C_{pv}} \tag{10}$$

In addition, the MOSFET voltage (v_M) and diode current (i_D) are

$$v_M = v_i \tag{11}$$

$$i_D = i_o = i_1 + i_2 \tag{12}$$

2.3. Waveforms Analysis

Figure 4 shows the waveforms of the different variables in the PV system based on the CIOC buck converter, where T is the switching period. These waveforms are constructed using the equations previously obtained in Sections 2.1 and 2.2 for the two topologies occurring during the PV system operation. The waveform of the L_1 current (i_1), which is the input current of the converter, confirms that the CIOC buck converter requests continuous current to the input capacitor. This is observed in the waveform of input capacitor current ($i_{C_{pv}}$), which is also continuous, and it is centered in zero due to the charge balance principle [29]. This characteristic ensures a smaller input capacitance requirement in comparison with converters imposing discontinuous capacitor currents, such as the classical buck structure.

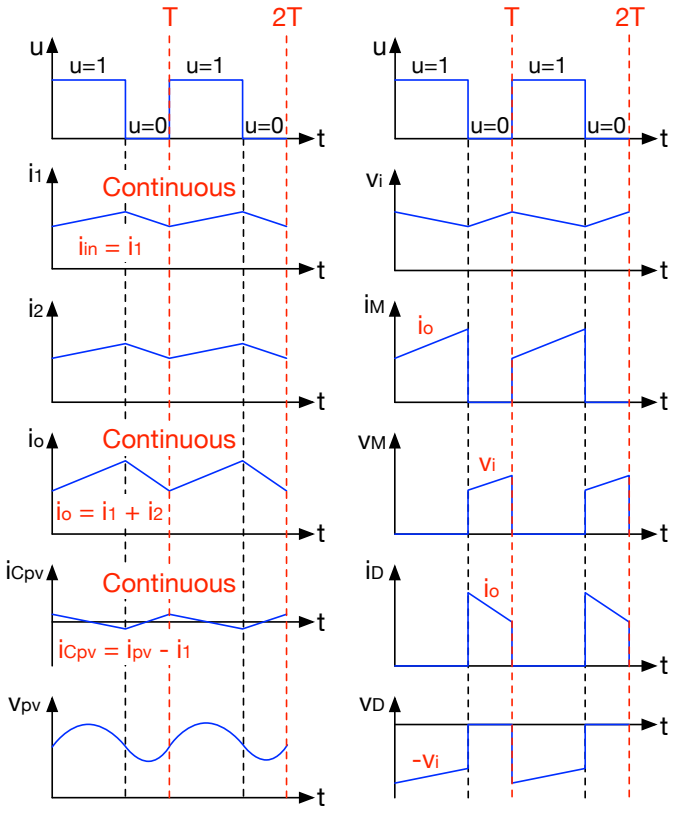

Figure 4. Waveforms of the PV system based on the CIOC buck converter.

The waveform of the PV voltage is obtained by integrating $i_{C_{pv}}$, which results in a second-order ripple, as reported in [29], due to the triangular shape of $i_{C_{pv}}$. In contrast, the waveform of the voltage v_i at the intermediate capacitor is triangular, this is because such a capacitor forms a first-order filter [29]. The current in L_2 (i_2) is also triangular, and it is in phase with i_2. Therefore, the output current $i_o = i_1 + i_2$ is continuous, and it exhibits a ripple equal to the sum of both current ripples.

Finally, in topology 1 ($u = 1$), the output current is transferred to the load using the MOSFET, thus the MOSFET current (i_M) is a discontinuous waveform with a peak current equal to i_o. Similarly, the output current is transferred to the load using the diode during topology 0 ($u = 0$); thus, the diode current (i_D) is a complementary discontinuous waveform with the same peak current. Finally, the MOSFET voltage (v_M) is equal to v_i when $u = 0$, while the diode voltage (v_D) is equal to $-v_i$ when $u = 1$.

In conclusion, both the input and output currents of the CIOC buck converter are continuous, which reduces the input capacitor of the PV system and provides a better power quality to the load in comparison with converters imposing discontinuous currents. This conclusion is further supported by a detailed comparison with a PV system based on a classical buck converter, which is given in Section 4.

3. Mathematical Model of the PV System Based on the CIOC Buck Converter

The elements and controller design of the PV system based on the CIOC buck converter require mathematical models with different characteristics. The first modeling approach, named switched model, is based on the differential equations obtained in Sections 2.1 and 2.2.

The switched differential equations modeling the inductor currents and capacitors voltages include the binary control signal u, which defines the effective equations for each topology:

$$\frac{di_1}{dt} = \frac{v_{pv} - v_o - v_i \cdot (1-u)}{L_1} \tag{13}$$

$$\frac{di_2}{dt} = \frac{v_i \cdot u - v_o}{L_2} \tag{14}$$

$$\frac{dv_i}{dt} = \frac{i_1 \cdot (1-u) - i_2 \cdot u}{C_i} \tag{15}$$

$$\frac{dv_{pv}}{dt} = \frac{i_{pv} - i_1}{C_{pv}} \tag{16}$$

Similarly, the current and voltages of both the MOSFET and diode are

$$i_M = (i_1 + i_2) \cdot u \tag{17}$$

$$v_M = v_i \cdot (1-u) \tag{18}$$

$$i_D = (i_1 + i_2) \cdot (1-u) \tag{19}$$

$$v_D = -v_i \cdot u \tag{20}$$

The previous model is useful to design nonlinear controllers with binary control signals, which is the case of the sliding-mode controller (SMC) designed in Section 5, to ensure a stable operation of the PV system.

A second modeling approach, named averaged model, is used to design controllers with continuous control signals, such as the duty cycle d. Moreover, the averaged model is used to analyze the closed-loop dynamics of dc/dc converters, which is the case of the closed-loop analysis performed in Section 5.4. The averaged model is obtained by averaging the switched differential equations within the switching period T, this taking

into account that the duty cycle is the average value of the MOSFET control signal u, as reported in Equation (21).

$$d = \frac{1}{T} \cdot \int_0^T u \, dt \tag{21}$$

Then, applying the same averaging technique for Equations (13) to (16) results in the following averaged differential equations:

$$\frac{di_1}{dt} = \frac{v_{pv} - v_o - v_i \cdot (1-d)}{L_1} \tag{22}$$

$$\frac{di_2}{dt} = \frac{v_i \cdot d - v_o}{L_2} \tag{23}$$

$$\frac{dv_i}{dt} = \frac{i_1 \cdot (1-d) - i_2 \cdot d}{C_i} \tag{24}$$

$$\frac{dv_{pv}}{dt} = \frac{i_{pv} - i_1}{C_{pv}} \tag{25}$$

Applying the same averaging technique for (17) to (20) results in the averaged equations for the currents and voltages of both the MOSFET and diode:

$$i_M = (i_1 + i_2) \cdot d \tag{26}$$

$$v_M = v_i \cdot (1-d) \tag{27}$$

$$i_D = (i_1 + i_2) \cdot (1-d) \tag{28}$$

$$v_D = -v_i \cdot d \tag{29}$$

The third modeling approach consists in obtaining the steady-state values of the inductors currents, capacitors voltages, and duty cycle. This approach is useful to design the passive elements of the PV system and to select the MOSFET and diode according the current and voltage stresses. The steady-state equations are calculated by considering the averaged differential equations equal to zero:

$$v_i = v_{pv} \tag{30}$$

$$i_2 = i_1 \cdot \frac{1-d}{d} \tag{31}$$

$$i_{pv} = i_1 \tag{32}$$

$$v_{pv} = \frac{v_o}{d} \tag{33}$$

$$d = \frac{v_o}{v_{pv}} = \frac{i_1}{i_1 + i_2} \tag{34}$$

It is important to note that the duty cycle (34) is the same one required by the classical buck converter; thus, the CIOC buck converter can be used to replace classical buck converters in PV systems.

In addition, the ripple values are also needed to design both the converter and SMC. These ripples are obtained from the differential equations for each topology given in Sections 2.1 and 2.2. For example, the current ripple in i_1 is obtained in topology 1 from (1), as given in (35). Similarly, the current ripple in i_2 is obtained in the same topology as given

in (36). Taking into account that $i_o = i_1 + i_2$, and that i_1 and i_2 are in phase, the ripple in the output current is calculated as given in (37).

$$\delta i_1 = \frac{v_{pv} \cdot d \cdot (1-d) \cdot T}{2 \cdot L_1} \tag{35}$$

$$\delta i_2 = \frac{v_{pv} \cdot d \cdot (1-d) \cdot T}{2 \cdot L_2} \tag{36}$$

$$\delta i_o = \frac{v_{pv} \cdot d \cdot (1-d) \cdot T}{2} \cdot \left(\frac{1}{L_1} + \frac{1}{L_2} \right) \tag{37}$$

The voltage ripple of C_i is also calculated in topology 0 from (9), as given in (38). Instead, the ripple at the PV voltage is calculated using the second-order filter procedure given in [29], where the current ripple in i_1 is integrated and the charge balance in C_{pv} is applied, thus obtaining the expression given in (39).

$$\delta v_i = \frac{i_{pv} \cdot (1-d) \cdot T}{2 \cdot C_i} \tag{38}$$

$$\delta v_{pv} = \frac{v_{pv} \cdot d \cdot (1-d) \cdot T^2}{16 \cdot C_{pv} \cdot L_1} \tag{39}$$

4. Comparison with a PV System Based on the Classical Buck Converter

Taking into account that the proposed PV system based on the CIOC buck converter has the same duty cycle as the classical buck converter, it is a suitable candidate to reduce the input capacitor of step-down PV systems. However, the CIOC buck converter has two inductors and two capacitors; thus, it is required to compare the inductive and capacitive requirements of both buck converters to provide a selection criterion.

The scheme of a PV system based on the classical buck converter is reported in Figure 5, where the PV source is interfaced using a capacitor which must filter the discontinuous input current generated by the MOSFET. Moreover, in the classical buck converter, the inductor current is the output current provided to the load.

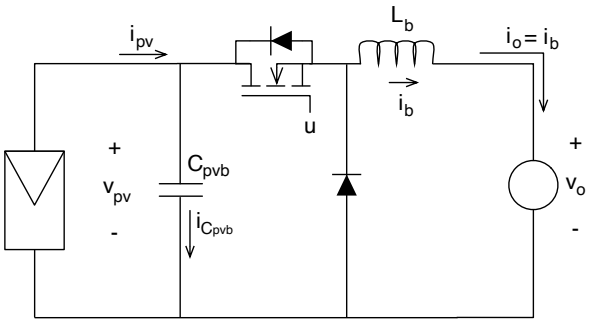

Figure 5. PV system based on the classical buck converter

The mathematical model of this PV system based on the classical buck converter is given in (40) and (41), where u is the control signal of the MOSFET, i_b is the current in the buck inductor L_b, and C_{pvb} is the input capacitance. The current and voltage of the

MOSFET are i_{Mb} and v_{Mb}, respectively, while the current and voltage of the diode are i_{Db} and v_{Db}, respectively.

$$\frac{di_b}{dt} = \frac{v_{pv} \cdot u - v_o}{L_b} \tag{40}$$

$$\frac{dv_{pv}}{dt} = \frac{i_{pv} - i_b \cdot u}{C_{pvb}} \tag{41}$$

$$i_{Mb} = i_b \cdot u \tag{42}$$

$$v_{Mb} = v_{pv} \cdot (1 - u) \tag{43}$$

$$i_{Db} = i_b \cdot (1 - u) \tag{44}$$

$$v_{Db} = -v_{pv} \cdot u \tag{45}$$

Performing the averaging procedure and making the differential equations equal to zero leads to the steady-state relations given in (46) and (47). Moreover, the inductor current ripple δi_b and PV voltage ripple δv_{pv} are given in (48) and (49), respectively.

$$d = \frac{v_o}{v_{pv}} \tag{46}$$

$$i_b = \frac{i_{pv}}{d} \tag{47}$$

$$\delta i_b = \frac{v_{pv} \cdot d \cdot (1 - d) \cdot T}{2 \cdot L_b} \tag{48}$$

$$\delta v_{pv} = \frac{i_{pv} \cdot (1 - d) \cdot T}{2 \cdot C_{pvb}} \tag{49}$$

In order to provide a fair comparison between both CIOC and classical buck converters, both converters must be designed to provide the same voltage ripple to the PV source and the same current ripple to the load (inverter). Considering both inductors of the CIOC converter are equal, thus $L_1 = L_2$, the output current ripple of the PV system is given in (50). The output ripple current in a PV system based on the classical buck converter was previously reported in (48); to obtain the same ripple magnitude in both PV systems, the classical buck solution must have half the inductance of the CIOC converter, hence $L_b = L_1/2$.

$$\delta i_o = \frac{v_{pv} \cdot d \cdot (1 - d) \cdot T}{L_1} \tag{50}$$

However, the inductor of the classical buck converter must support a higher current in comparison with the inductors of the CIOC converter, which is concluded from (31), (32), and (47). Therefore, a better measurement to compare the inductive requirements of both converters is the energy stored in the inductors: for example, for a duty cycle $d = 0.5$, the inductor of the classical buck converter stores $E_{L,b} = \frac{1}{2} \cdot L_b \cdot i_b^2 = 2 \cdot L_b \cdot i_{pv}^2$, since $i_b = 2 \cdot i_{pv}$, as given in (47). Taking into account that $L_b = L_1/2$ to ensure the same output current ripple in both converters, the energy stored in the classical buck inductor becomes $E_{L,b} = L_1 \cdot i_{pv}^2$. For the same duty cycle $d = 0.5$, the energy stored in each of the CIOC inductors is $E_1 = \frac{1}{2} \cdot L_1 \cdot i_{pv}^2$, since $i_1 = i_{pv}$, as given in (32). Therefore, the total energy stored in both CIOC inductors is $E_{L,CIOC} = L_1 \cdot i_{pv}^2$, which is the same energy stored in the single inductor of the classical buck converter. In conclusion, both converters have the same inductive requirements (in terms of stored energy) to provide the same output current ripple.

Concerning the PV voltage ripple, making equal the ripple Equations (39) and (49) with $L_b = L_1/2$ leads to the relation needed between the input capacitor of the classical

buck converter C_{pvb} and the input capacitor of the CIOC buck converter C_{pv} to obtain the same ripple:

$$\frac{C_{pvb}}{C_{pv}} = \frac{8 \cdot i_{pv} \cdot L_1}{v_o \cdot T} \tag{51}$$

To illustrate the previous relation, an inductor of $L_1 = 38$ µH is considered. Moreover, an output voltage for both PV system $v_o = 24$ V and a switching frequency equal to 93 kHz ($T = 10.8$ µs) are assumed for the comparison. Under those conditions, the classical buck converter requires an input capacitor almost 12 times higher than the CIOC converter. However, in this case, both capacitors have the same voltage, thus the energy stored in the input capacitor of the classical buck converter is 12 times higher than the energy stored in the input capacitor of the CIOC converter.

An additional comparison between both converters is provided in Figure 6, where variations on the inductance, switching period, and output voltage are considered. These comparisons show that reducing the inductance also reduces the difference in the capacitance requirements, but at the expense of increasing the output current ripple. Similarly, increasing the switching period also reduces the difference in the capacitance requirements and increases the output current ripple. Finally, increasing the output voltage reduces the difference in the capacitance requirements, but the output voltage is defined by the load, thus it is not a freedom degree. In any case, it is important to note that in small output voltages the proposed PV system requires a much smaller input capacitor.

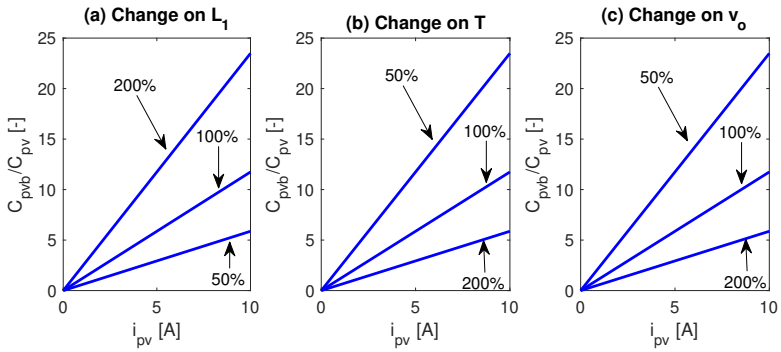

Figure 6. Input capacitor comparison between both buck converters.

In conclusion, for the same PV voltage ripple condition, the CIOC PV system has a much lower capacitance requirement in comparison with a PV system based on the classical buck converter. It is noted that the CIOC PV system requires an additional intermediate capacitor C_i, but such a capacitor is smaller than the main capacitor C_{pv} because the C_i current is defined by the inductor currents; this condition is illustrated in Section 7.

5. Sliding-Mode Controller for Maximum Power Point Tracking

The correct operation of the PV system requires the tracking of the optimal operating condition for a particular irradiance and temperature reaching the PV source. Several algorithms have been designed to track the maximum power point (MPP), in which the PV source produces the maximum power [48]. The proposed PV system based on the CIOC converter can operate with any of these maximum power point tracking (MPPT) algorithms; however, the most widely adopted MPPT solution is the perturb and observe (P&O) algorithm, which is described in [49]. Therefore, this section considers the P&O algorithm parameters to design the controller for the CIOC converter, but any other MPPT algorithm can be used.

The P&O algorithm is a hill-climbing optimization technique [46]; thus, the manipulated variable is perturbed to detect the direction in which the objective variable is optimized. In the case of PV systems, the manipulated variable to be optimized is the

voltage at the PV source v_{pv}, and the objective variable to be maximized is the PV power p_{pv}. Therefore, the input voltage v_{pv} of the CIOC converter must be regulated to follow the reference provided by the *P&O* algorithm, which in this paper is named v_{MPPT}. This regulation is performed using a sliding-mode controller (SMC) to provide global stability.

5.1. Definition of the Switching Function and Transversality Analysis

The first step to design an SMC is to design the desired dynamic of the system, which is expressed as a switching function defining the system trajectory. Taking into account the control objective $v_{pv} = v_r$, where v_r is the controller reference, the obvious switching function Ψ_v is given in (52), where the desired surface is $\Psi_v = 0$.

$$\Psi_v = v_r - v_{pv} \tag{52}$$

However, the switching function is usable only if three conditions are fulfilled, as demonstrated in [50,51]:

- Transversality condition, which evaluates the presence of the control variable into the switching function derivative. This condition is mandatory, otherwise the SMC will not be able to modify the trajectory of the CIOC converter. In this case, the control signal u defines the activation/deactivation of the MOSFET and diode. The transversality condition is formalized as follows:

$$\frac{d}{du}\left(\frac{d\Psi}{dt}\right) \neq 0 \tag{53}$$

- Reachability conditions, which evaluate the ability to reach the desired operating condition from any starting point. This condition is mandatory to compensate any perturbation of the system. In this case, the perturbations are introduced by changes on the solar irradiance, or by changes in the load voltage and/or impedance.
- Equivalent control condition, which evaluates that the average value of the control signal u is always trapped inside the control variable limits; i.e., evaluating the saturation of the average value. In dc/dc converters, the average value of the control signal corresponds to the duty cycle (21), hence the equivalent control condition evaluates that the duty cycle is never saturated. This is important since a dc/dc converter with saturated duty cycle operates in open loop, thus nullifying the control action.

In addition to the previous three conditions, the closed-loop dynamics of the SMC must be analyzed to ensure that the desired performance is achieved.

Performing the transversality analysis to the switching function Ψ_v requires the calculation of that function derivative, which is given in (54). Then, applying the transversality test defined in (53) results in $\frac{d}{du}\left(\frac{d\Psi}{dt}\right) = 0$, since u is not present in Equation (54); thus, the switching function (52) does not fulfill the transversality condition, and it is not suitable to design an SMC.

$$\frac{d\Psi_v}{dt} = \frac{dv_r}{dt} - \frac{i_{pv} - i_1}{C_{pv}} \tag{54}$$

The next option is to include the derivative of the objective variable into the switching function, which could enable to modify the system trajectory. In this case, the derivative of the PV voltage can be obtained from measuring the input capacitor current, since $i_{C_{pv}} = C_{pv} \cdot \frac{dv_{pv}}{dt}$. In addition, the new sliding function will include the integral of the voltage error to ensure a correct tracking of the reference. Finally, the components of the new switching function Ψ are weighted using the constants k_p, k_i, and k_c as follows:

$$\Psi = k_p \cdot (v_r - v_{pv}) + k_i \cdot \int (v_r - v_{pv})\, dt + k_c \cdot i_{C_{pv}} \tag{55}$$

The derivative of this new switching function is given in (56), and applying the transversality test (53) leads to expression (57), which confirms that the transversality condition is fulfilled, because $k_c \neq 0$ is needed to include the input current measurement.

$$\frac{d\Psi}{dt} = k_p \cdot \frac{dv_r}{dt} - k_v \cdot \frac{i_{pv} - i_1}{C_{pv}} + k_i \cdot (v_r - v_{pv}) + k_c \cdot \frac{di_{pv}}{dt} - k_c \cdot \frac{v_{pv} - v_o - v_i \cdot (1-u)}{L_1} \quad (56)$$

$$\frac{d}{du}\left(\frac{d\Psi}{dt}\right) = -k_c \cdot \frac{v_i}{L_1} \neq 0 \quad (57)$$

In conclusion, the switching function (55) is a suitable option to design the SMC for the PV system based on the CIOC converter, where the surface is $\Psi = 0$. However, the sign of the transversality value (57) is needed to perform the analysis of the reachability conditions. In Section 5.4 it is demonstrated that parameter k_c must be negative ($k_c < 0$) to ensure stable closed-loop dynamics; thus, the sign of the transversality value (57) is positive.

5.2. Reachability Conditions

The reachability conditions evaluate the system capability to reach the surface:

- When the system is operating under the surface ($\Psi < 0$), the switching function derivative must be positive $\frac{d\Psi}{dt} > 0$ to reach the desired condition $\Psi = 0$. Taking into account that the transversality value (57) is positive, this means that a positive change on the control signal u (from 0 to 1) produces a positive change on $\frac{d\Psi}{dt}$; thus, this reachability condition is formalized as follows:

$$\lim_{\psi \to 0^-} \left.\frac{d\Psi}{dt}\right|_{u=1} > 0 \quad (58)$$

- When the system is operating above the surface ($\Psi > 0$), the switching function derivative must be negative $\frac{d\Psi}{dt} < 0$ to reach the desired condition $\Psi = 0$. Since (57) is positive, this means that a negative change on the control signal u (from 1 to 0) produces a negative change in $\frac{d\Psi}{dt}$; thus, this second reachability condition is formalized as follows:

$$\lim_{\psi \to 0^+} \left.\frac{d\Psi}{dt}\right|_{u=0} < 0 \quad (59)$$

Evaluating the previous theoretical reachability conditions, using the switching function derivative given in (56) leads to the following dynamic restrictions for the reference derivative $\frac{dv_r}{dt}$, which must be fulfilled to ensure both reachability conditions (58) and (59):

$$-\frac{k_c}{k_p} \cdot \left(\frac{di_{pv}}{dt} - \frac{v_{pv} - v_o}{L1}\right) - \frac{k_i}{k_p} \cdot \Delta v_{po} < \frac{dv_r}{dt} < -\frac{k_c}{k_p} \cdot \left(\frac{di_{pv}}{dt} + \frac{v_o}{L1}\right) - \frac{k_i}{k_p} \cdot \Delta v_{po} \quad (60)$$

The previous expression takes into account that the average value of v_{pv} is equal to the average value of v_i, as demonstrated in (30); in addition, it also takes into account that the average value of i_{pv} is equal to the average value of i_1, as demonstrated in (32). Moreover, since the reference v_r is defined by a P&O algorithm, each perturbation in the reference has a magnitude equal to the P&O perturbation parameter Δv_{po}, thus $\Delta v_{po} = v_r - v_{pv}$.

In conclusion, the dynamic behavior of the reference signal must be constrained as given in (60) to ensure that both reachability conditions are always fulfilled.

5.3. Equivalent Control Condition

The analysis of the equivalent control condition requires to calculate the average value of the control signal u, which is equal to the duty cycle, as given in (21). This analysis, which evaluates the saturation of the duty cycle, is performed when the system is operating

into the sliding surface, thus $\Psi = 0$ and $\frac{d\Psi}{dt} = 0$. Then, using the expression of $\frac{d\Psi}{dt}$ given in (56) at the condition $\frac{d\Psi}{dt} = 0$ leads to the following expression for the duty cycle:

$$d = \frac{L_1}{k_c \cdot v_i} \cdot \left(k_p \cdot \frac{dv_r}{dt} + k_c \cdot \frac{di_{pv}}{dt} + k_c \frac{v_o}{L_1} + k_i \cdot \Delta v_{po} \right) \tag{61}$$

Then, the equivalent control condition is $0 < d < 1$, and introducing the d value obtained in (61) leads to the same dynamic restriction obtained from the reachability conditions, which was reported in (60). Therefore, fulfilling the dynamic restriction given in (60) ensures that both reachability and equivalent control conditions are true, hence ensuring the global stability of the PV system based on the CIOC converter.

5.4. Closed-Loop Dynamics and Controller Parameters

The closed-loop operation of the PV system is analyzed considering a correct operation of the SMC; hence, it is assumed that the switching function (55) is inside the sliding surface $\Psi = 0$. Therefore, the SMC imposes the following current-to-input capacitor C_{pv}:

$$i_{C_{pv}} = -\frac{k_p \cdot (v_r - v_{pv}) + k_i \cdot \int (v_r - v_{pv})\, dt}{k_c} \tag{62}$$

Considering that $i_{C_{pv}} = C_{pv} \cdot \frac{dv_{pv}}{dt}$ and applying the Laplace transformation leads to the following expression for the closed-loop dynamics of the PV voltage:

$$\frac{v_{pv}}{v_r} = \frac{k_p \cdot s + k_i}{-k_c \cdot C_{pv} \cdot s^2 + k_p \cdot s + k_i} \tag{63}$$

From the Routh–Hurwitz stability criterion [52], it is known that all coefficients of the previous transfer function must be positive to ensure that both equivalent poles are at the left-hand plane (LHP) of the Laplace space, thus ensuring a stable closed-loop operation, as anticipated in Section 5.1. Therefore, the following conditions must be fulfilled: $k_c < 0$, $k_p > 0$ and $k_i > 0$. The equivalent poles of the closed-loop transfer function are given in (64), where the pole values depend on the relations k_p/k_c and k_i/k_c. Hence, the k_c value given in (65) is defined to ensure the negative sign.

$$s = \frac{1}{2} \cdot \left[\frac{k_p/k_c}{C_{pv}} \pm \sqrt{\left(\frac{k_p/k_c}{C_{pv}} \right)^2 + \frac{4 \cdot k_i/k_c}{C_{pv}}} \right] \tag{64}$$

$$k_c = -1 \tag{65}$$

The other two parameters of the SMC (k_p and k_i) must be designed to ensure stable operation of the P&O algorithm. In [46,47], it was demonstrated that the settling time t_s of the PV voltage v_{pv} must be shorter than the perturbation period T_{po} of the P&O algorithm, otherwise the system becomes unstable. This stability condition ($t_s < T_{po}$) is simple to explain: the P&O algorithm perturbs the PV voltage v_{pv} to observe the direction in which the PV power p_{pv} is increased; therefore, the PV voltage must be stable to perform a correct observation of the PV power. Instead, if the PV voltage is not stable, the observed PV power will be a transient value; thus, it could produce a wrong decision, making the operation of the P&O algorithm unstable. In conclusion, the SMC must ensure that the settling time t_s of the PV voltage is correct, i.e., $t_s < T_{po}$.

The reference signal provided by the P&O algorithm is a series of perturbations with magnitude Δv_{po} each T_a seconds, which is explained in detail in [46,49]; hence, the reference signal v_r of the SMC can be modeled as a step waveform with magnitude Δv_{po}, which is represented in the Laplace domain as follows:

$$v_r = \frac{\Delta v_{po}}{s} \tag{66}$$

The time response of the PV voltage to the perturbation of the P&O algorithm is obtained by calculating the inverse Laplace transformation of the multiplication of transfer function (63) by reference signal (66). For this process, it is imposed to (63) a damping factor $\rho = 1$, which provides a PV voltage waveform with low overshoots. Contrasting the denominator coefficients of (63) with the canonical form $s^2 + 2 \cdot \rho\omega_n \cdot s + \omega_n^2$, for a defined $\rho = 1$ condition, leads to the k_i value given in (67). Using such a k_i value, the time response of the PV voltage is given in (68).

$$k_i = \frac{k_p^2}{4 \cdot C_{pv}} \tag{67}$$

$$v_{pv} = \Delta v_{po} \cdot \left[1 - e^{-k_p \cdot t/\left(2 \cdot C_{pv}\right)} + \frac{k_p \cdot t}{2 \cdot C_{pv}} \cdot e^{-k_p \cdot t/\left(2 \cdot C_{pv}\right)}\right] \tag{68}$$

The settling time t_s is calculated when the PV voltage enters an acceptable band, which in this case is selected as $\epsilon = 1\%$. Then, solving Equation (68) for $v_{pv} = 1 + \epsilon$ results in the settling time expression given in (69), which is used to obtain the value of k_p, given in (70), which is needed to ensure the desired settling time t_s value.

$$t_s = 2 \cdot C_{pv} \cdot \frac{1 - W\left(-\epsilon \cdot e^1\right)}{k_p} \tag{69}$$

$$k_p = \frac{2 \cdot C_{pv}}{t_s} \cdot \left[1 - W\left(-\epsilon \cdot e^1\right)\right] \tag{70}$$

5.5. Hysteresis Band and Switching Frequency

The main inconvenience of the sliding-mode control technique is the high switching frequency imposed by the controller:

- Stage 1: When $\Psi < 0$, the first reachability condition (58) imposes the control action $u = 1$, which forces the increment of the switching function Ψ towards $\Psi = 0$. However, when Ψ reaches 0, there is no change in the control action, thus Ψ is further increased into $\Psi > 0$ (Stage 2).
- Stage 2: When $\Psi > 0$, the first reachability condition (59) imposes the control action $u = 0$, which forces the decrement in the switching function Ψ towards $\Psi = 0$. However, as in Stage 1, there is no change in the control action when when $\Psi = 0$, thus Ψ is further decreased into $\Psi > 0$ (Stage 1).
- In this theoretical operation, transition time between Stage 1 and Stage 2 is only limited by the time required by the MOSFETs and diodes to open and close.

However, MOSFET and diodes have transition times recommended for correct operation which are much longer than the maximum transition times physically achievable. Thus, operating those semiconductors at higher switching frequencies (than the recommended ones) reduces the semiconductors lifetime and significantly increase the power losses.

Therefore, the practical implementation of SMC considers the introduction of hysteresis bands around the sliding surface, which makes it possible to limit the switching frequency to be in agreement with the requirements of the semiconductors. In this way, the practical sliding surface is formalized, as given in (71), and the associated practical reachability conditions are formalized in expression (72).

$$-H \leq \Psi \leq +H \tag{71}$$

$$\lim_{\psi \to -H^-} \left.\frac{d\Psi}{dt}\right|_{u=1} > 0 \ \wedge \ \lim_{\psi \to +H^+} \left.\frac{d\Psi}{dt}\right|_{u=0} < 0 \tag{72}$$

These practical reachability conditions impose the control law to be used in the SMC implementation, which is formalized as follows:

$$\left\{ \begin{array}{l} \text{if } \Psi < -H \ \rightarrow \ \text{set } u = 1 \\ \text{if } \Psi > +H \ \rightarrow \ \text{set } u = 0 \end{array} \right\} \tag{73}$$

The maximum switching frequency of this practical implementation is defined by the time that it takes the switching function to travel between the hysteresis limits, i.e., from $-H$ to $+H$, which corresponds to the ripple of the switching function. Therefore, the ripple of the switching function is equal to the hysteresis limit H.

The analysis of the ripple H is performed using the ripple of the variables forming the switching function $\Psi = k_p \cdot \left(v_r - v_{pv}\right) + k_i \cdot \int \left(v_r - v_{pv}\right) \, dt + k_c \cdot i_{C_{pv}}$, which are the PV voltage v_{pv} and input capacitor current $i_{C_{pv}}$. Taking into account that the correct operation of the SMC ensures that $v_{pv} = v_r$, the ripple of the term $k_p \cdot \left(v_r - v_{pv}\right)$ is equal to the ripple of the PV voltage multiplied by k_p, i.e., $-k_p \cdot \delta v_{pv(t)}$. Moreover, the charge balance principle [29] ensures that the average current in the input capacitor is equal to zero, hence the ripple of the term $k_c \cdot i_{C_{pv}}$ is equal to the ripple in the inductor current multiplied by k_c, i.e., $k_c \cdot \delta i_{1(t)}$. Finally, since the ripple at the PV voltage is symmetrical with respect to the average value, the ripple of the term $k_i \cdot \int \left(v_r - v_{pv}\right) \, dt$ is equal to zero. The previous analyses are synthesized as follows:

$$H = \left| -k_p \cdot \delta v_{pv(t)} + k_c \cdot \delta i_{1(t)} \right| \tag{74}$$

From Figure 4, it is observed that the ripple waveforms of $i_{C_{pv}}$ and v_{pv} are phase-shifted in 90°, hence the maximum value of the voltage ripple in v_{pv} occurs when the ripple of $i_{C_{pv}}$ is zero, and the maximum value of the ripple in $i_{C_{pv}}$ occurs when the ripple in v_{pv} is zero (v_{pv} equal to the average value). In conclusion, the ripple H of Ψ is equal to the maximum component as follows:

$$H = \max\left(\left| -k_p \cdot \delta v_{pv} \right|, \left| k_c \cdot \delta i_1 \right| \right) \tag{75}$$

The previous equation is combined with the expressions for δi_1, given in (35), and δv_{pv}, given in (39), to calculate the H value that ensures the desired maximum switching frequency $F = 1/T$, which is defined in agreement with the characteristics of the MOSFET and diode selected for the implementation.

5.6. SMC Implementation

The controller (SMC) implementation is divided in two parts: first, the switching function Ψ (55) must be calculated; second, the control law (73) must be implemented. Figure 7 shows the block diagram for the SMC implementation, where the calculation of the switching function is based on linear elements such as adders, static gains, and an integrator. These linear blocks are constructed using operational amplifiers, as it is shown in the circuital implementation described aftewards. The control law is implemented using two comparators for the $\Psi < -H$ and $\Psi > +H$ operations, as well as an SR flip-flop for the set $u = 1$ and set $u = 0$ operations, where the last one corresponds to the reset condition of the flip-flop.

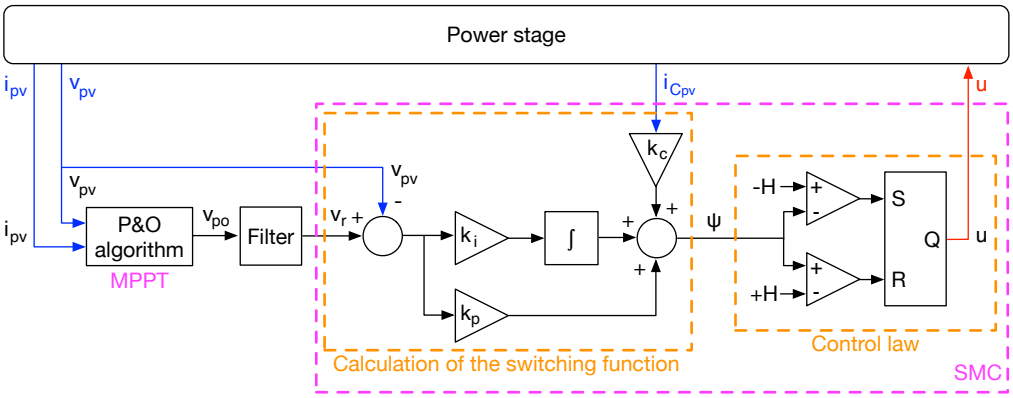

Figure 7. Block diagram of the proposed SMC (measured signals: blue lines; control signal: red line).

The block diagram also shows the connection of the P&O algorithm, where a filter is inserted between the MPPT block and the SMC. That filter is needed to ensure that the dynamic restriction (60), imposed by the reachability conditions, is fulfilled. The filter is implemented using the first-order transfer function given in (76), where the time constant of the filter τ_f must be calculated in agreement with the restrictions for $\frac{dv_r}{dt}$.

$$\frac{v_r}{v_{po}} = \frac{1}{\tau_f \cdot s + 1} \tag{76}$$

The time response of the filter is (77), where the maximum derivative occurs at $t = 0$. Therefore, the time constant of the filter needed to ensure a desired maximum derivative (*Rate*) is given in (78).

$$v_r = \Delta v_{po} \cdot \left(1 - e^{-t/\tau_f}\right) \tag{77}$$

$$\tau_f = \frac{\Delta v_{po}}{Rate} \tag{78}$$

Finally, since this first-order filter imposes the same derivative limitation to both positive and negative changes, the *Rate* value must be selected to be equal to the limit of (60) with lower magnitude. This will ensure that both dynamic restrictions are always fulfilled, thus ensuring the SMC stability.

6. Design Procedure and Application Example

This section synthesizes the design procedure of the proposed PV solution using an application example based on the SP500M6-96 PV panel [53] and the commercial inverter COTEK SP-700-124 [8], which is a 700 W inverter with a 24 V input and a single-phase ac output of 100, 110, 115, or 120 V and 50 or 60 Hz. However, both grid-connected inverters and off-grid inverters produce the inverter input oscillations at twice the output frequency. The characteristics of both the panel and pure sine wave inverter are given in Table 1. Although a pure sine wave off-grid inverter is used in the application example, a grid-connected inverter also could be used with the CIOC. A commercial example of a grid-connected inverter is presented in [11], where the inverter input voltage is between 19 V and 33 V, and the PV array maximum voltage is 250 V; moreover, this particular inverter also has an input for a battery bank with a nominal voltage of 24 V and can be connected to a grid of 230 V of 50 Hz.

Table 1. Parameters of the SP500M6-96 PV panel and COTEK SP-700-124 inverter.

Parameter	Value
Panel maximum Power (P_{mpp})	500 W
Panel maximum power voltage (V_{mpp})	48.63 V
Panel maximum power current (I_{mpp})	10.28 A
Panel short-circuit current (I_{sc})	10.87 A
Panel open-circuit voltage (V_{oc})	58.95 V
Inverter input voltage range (v_o)	21–33 V
Inverter nominal output voltage (RMS)	100/110/115/120 V
Inverter nominal output power	700 W
Inverter output frequency	50/60 Hz

The electrical characteristics of the SP500M6-96 PV panel are presented in Figure 8, where the current vs. voltage (I-V) and power vs. voltage (P-V) curves are observed for different irradiance (S) conditions. The figure also shows the trajectory of the maximum power points (MPP) of the PV panel, which corresponds to the trajectory where the PV system must be operated.

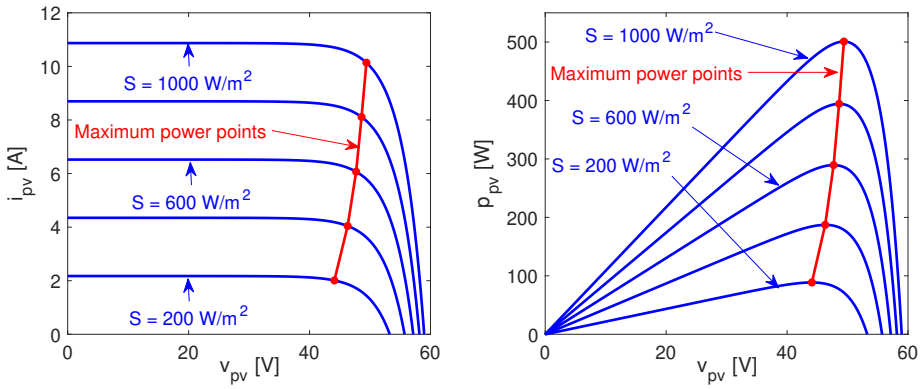

Figure 8. Electrical characteristics of the SP500M6-96 PV panel.

The first step is to design the inductors of the CIOC converter. Since the ripple δi_o of the output current (37) depends on the inverse of both inductors, these inductors are designed equally to share the ripple balanced between both i_1 and i_2 currents, thus $L_1 = L_2$. In addition, the switching frequency is limited to 100 kHz to enable the use of standard (and cheap) power MOSFET and diodes, such as CSD19538Q3A [54] and V15P8 [55], respectively; hence, $F \leq 100$ kHz. From the electrical characteristics reported in Figure 8, it is observed that the PV source provides 88.5 W at $S = 200$ W/m^2, which imposes an output current of the CIOC converter (delivered to the load at 24 V) equal to 3.69 A; hence, the output current ripple at $S = 200$ W/m^2 must be $\delta i_o \leq 3.69$ A to ensure continuous conduction mode (CCM) in the CIOC converter for $S \geq 200$ W/m^2. The design procedure could be performed for a lower irradiance limit, but the small current value, thus small current ripple, will introduce negligible harmonics that will not justify the increment in the inductances. Based on the previous values, Equation (75) is used to calculate the switching frequency for different inductance values for the irradiance range 200 W/m^2 $\leq S \leq$ 1000 W/m^2, where the data for $S = 1000$ W/m^2 corresponds to the MPP conditions reported in Table 1. Figure 9 depicts the results of Equation (75), where the value $L_1 = L_2 =$ 38 µH is selected to ensure the desired $F \leq 100$ kHz condition, since the Earth irradiance is always lower than 1000 W/m^2.

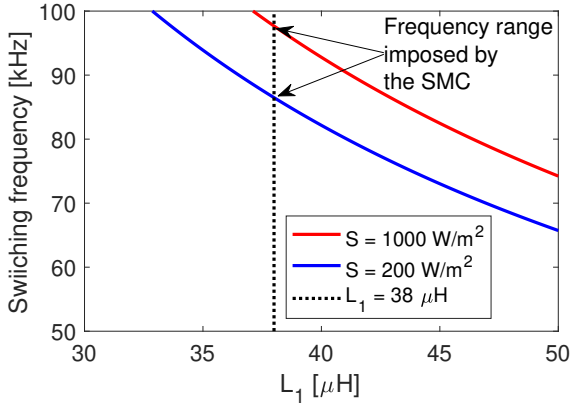

Figure 9. Design of the inductors in the CIOC converter.

The next step is to design the input capacitor C_{pv} in agreement with the requirements of the PV system. Taking into account that the P&O algorithm has an efficiency of 99% in tracking the MPP condition [49], the PV voltage ripple δv_{pv} must be lower than 1% of v_{mpp}. Therefore, the peak-to-peak amplitude of the PV ripple is defined as the 20% of such a 1% limit, hence δv_{pv} = 50.87 mV. Then, using expression (39) and the previous value of L_1 leads to the input capacitance value 42.88 µF, where the commercial value $C_{pv} = 47$ µF is selected. Concerning the internal capacitor (C_i), it is designed to ensure a CCM operation for 80% of the converter conditions: taking into account that $v_i = v_{pv}$, as given in (30), and the peak-to-peak voltage ripple in C_i is defined as 20% of v_{mpp}, thus δv_i = 4.94 V. Then, using Equation (38), the internal capacitance 5.54 µF is calculated, where the commercial value $C_i = 5.6$ µF is selected.

After the power stage parameters have been designed, the following step is to calculate the appropriate parameters for the controller (SMC). The first parameter was already designed in Equation (65), where $k_c = -1$. The other two parameters are calculated in agreement with the requirements of the P&O algorithm, which in turn is designed as described in [46,47]: the perturbation amplitude is designed as the 1% of the MPP voltage, thus Δv_{po} = 500 mV; the perturbation period is designed as $T_{po} = 500$ µs to provide a balance between processing requirements and tracking speed. Then, the settling time of the PV voltage is defined as 50% of the T_{po} parameter to ensure the P&O stability ($t_s < T_{po}$), thus $t_s = 250$ µs. Using Equation (70) and both the C_{pv} and t_s values leads to the calculation of the parameter k_p = 2.36 [A/V]; the remaining SMC parameter is calculated using Equation (67) as k_i = 29.5 [kA/ (V · s)].

The last part of the design concerns the stability filter. This application is designed to ensure global stability even under fast perturbations on the irradiance conditions, which is considered as one sun per millisecond or $\frac{dS}{dt}$ = 1000 W/(m^2· ms), which is translated into $\frac{di_{pv}}{dt}$ = 10.87 A/ms. This irradiance perturbation corresponds to a transition from full irradiance to complete shading (or vice-versa) in one millisecond, thus covering any practical perturbation. Using Equation (60) with the system parameters and the PV current perturbation leads to the maximum reference derivative $Rate$ = 0.257 V/µs accepted to ensure the SMC stability. Finally, from Equation (78), the filter time constant is calculated as τ_f = 1.95 µs, which is less than 20% of a single switching period of the CIOC converter; thus, it has a negligible effect on the settling time. The last parameter of the PV system is the hysteresis width, which is calculated from Equation (75) as H = 1.67 A. Table 2 summarizes the parameters of this application example used to illustrate the proposed design process.

Table 2. Design example of the PV system based on the CIOC converter.

Parameter	Value
L_1, L_2	38 [µH]
C_{pv}	47 [µF]
C_i	5.6 [µF]
$\max(F)$	100 [kHz]
Δv_{po}	500 [mV]
T_{po}	500 [µs]
t_s	250 [µs]
k_c	-1 [−]
k_p	2.36 [A/V]
k_i	29.5 [kA/(V · s)]
$Rate$	0.257 [V/µs]
τ_f	1.95 [µs]
H	1.67 [A]

Finally, Figure 10 synthesizes the proposed design process for the PV system based on the CIOC converter: the first part describes the converter design based on both the source and load characteristics, the second part concerns the MPPT algorithm design, and the third part is devoted to the controller (SMC) design to guarantee global stability.

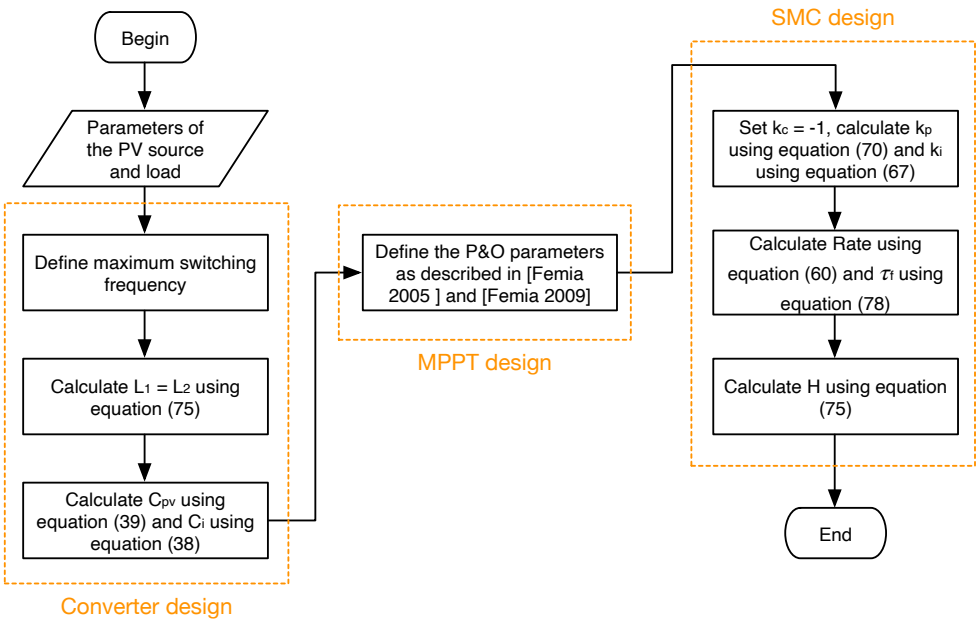

Figure 10. Flowchart of the proposed design process, where the P&O parameters are defined following [46,47].

7. Circuital Implementation and Simulations

The circuital implementation of the complete PV system based on the CIOC converter and the SMC was performed in the power electronics simulator PSIM [56]. Such a commercial power electronics simulator takes into account the nonlinear and switched behavior of both the MOSFET and diode, provides realistic models for operational amplifiers and flip-flops, and also enables the emulation of microcontrollers using ANSI C code. Figure 11 shows the proposed PV system implemented in the schematic editor of PSIM.

The PV source is implemented using the ideal single-diode model reported in [25], where the model equation is $i_{pv} = i_{sc} - A \cdot e^{B \cdot v_{pv}}$, and the parameters values for the SP500M6-96 PV panel are A = 642.9 nA and B = 0.2823 V^{-1}. The load is represented by a series connection of a DC source, which represents the average voltage imposed by the

inverter, as well as a sinusoidal component at double the output frequency, which models the voltage oscillation at double of the output frequency caused by the ac connection of a single-phase inverter. The amplitude of such a low-frequency oscillation was discussed in [57], and the mathematical analyses provided in such a work lead to expression (79), where f_g is the output frequency, C_{ac} is the capacitor at the input of the inverter, and $\langle v_o \rangle$ is the average voltage imposed by the inverter at the output of the CIOC converter. For the PV source and inverter parameters given in Table 1, a capacitor C_{ac} = 5.7 mF will produce a voltage oscillation between 21.6 V and 26.4 V, which fits the input voltage range required by the COTEK SP-700-224 inverter to properly operate (see Table 1). Thus, the maximum amplitude of the load voltage perturbations is equal to 20% of the nominal value (24 V).

$$\Delta v_o = \frac{p_{pv}}{4 \cdot \pi \cdot f_g \cdot C_{ac} \cdot \langle v_o \rangle} \tag{79}$$

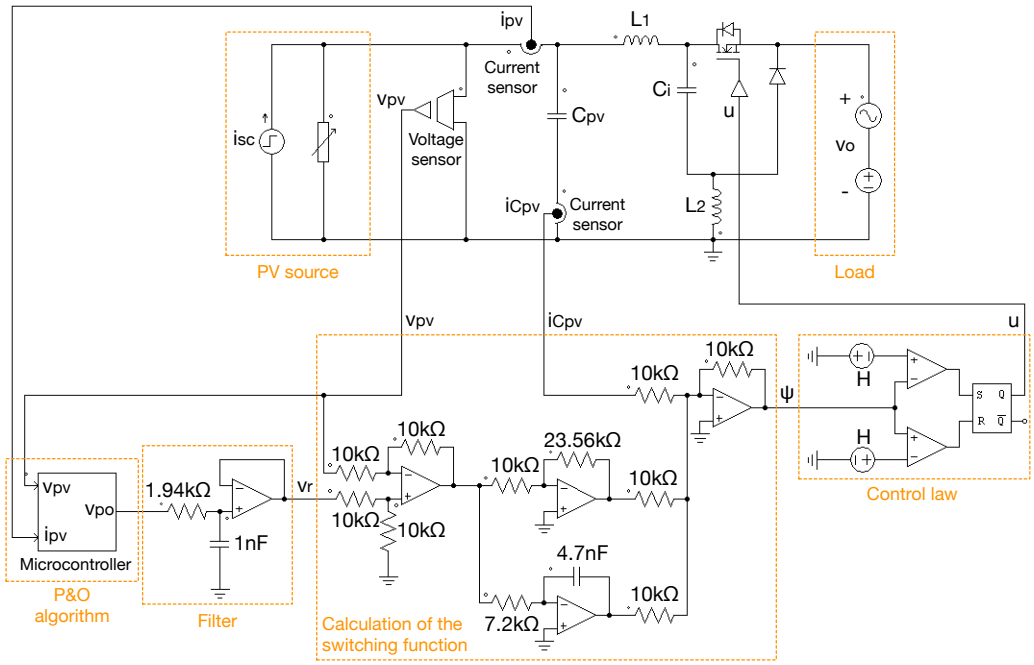

Figure 11. Circuital implementation of the PV system based on the CIOC converter and SMC.

The parameters of the CIOC converter are the same ones designed in the previous section and reported in Table 2. However, the circuit of Figure 11 includes one voltage sensor to measure the PV voltage, which is needed to process both the P&O algorithm and the calculation of the switching function. In addition, two current sensors are also added: the first one measures the PV current, which is needed to process the P&O algorithm, and the second one measures the input capacitor current, which is needed for the calculation of the switching function.

The circuital implementation of the control stage is divided into four parts. First, the P&O algorithm is coded using the algorithm reported in [49], which is implemented with a C-block inside PSIM to emulate a microcontroller. The second part implements the stability filter using an operational amplifier, and the third part performs the calculation of the switching function with circuits based on operational amplifiers. Finally, the fourth part implements the control law using two comparators and an SR flip-flop.

The first simulation compares the operation of the designed PV system based on the CIOC converter with a PV system based on the classical buck converter. The design of the buck PV system was discussed in Section 4, where the buck inductor and capacitor needed to match the PV voltage, and the output current ripples of the CIOC solution are L_b = 19 µH and C_{pvb} = 550 µF, respectively. Figure 12 shows the comparison of the PV

systems based on both the CIOC and the classical buck converters, where both solutions introduce the same PV voltage ripple (top traces), thus fulfilling the requirements of the MPPT algorithm. Moreover, both solutions also introduce the same current ripple into the load (second traces of Figure 12), hence providing the same power quality. However, the PV system based on the classical buck converter requires an input capacitor 11.7 times bigger than the capacitive requirement of the CIOC converter (the buck converter stores 11.7 times more energy), which introduces reliability problems, since bigger capacitances have higher failure rates [58]. This high capacitive condition of the buck converter is caused by the discontinuous input (MOSFET) current that must be filtered in the input capacitor: the current at the input capacitor $i_{C_{pv}} = i_{pv} - i_M$ is discontinuous for the buck-based PV system, which in this example corresponds to an RMS current equal to 10.51 A; instead, the CIOC input capacitor has a continuous current ($i_{C_{pv}} = i_{pv} - i_1$), thus the input capacitor must filter much lower current harmonics (RMS current equal to 1.01 A). Such a condition is confirmed in the third traces of Figure 12. Finally, despite the inductors of the CIOC converter having higher inductance, the current processed by these inductors is much lower, and the total energy stored in the inductors of the CIOC converter is the same energy stored in the single inductor of the buck converter; thus, the inductive requirements are equivalent, as it was demonstrated in Section 4.

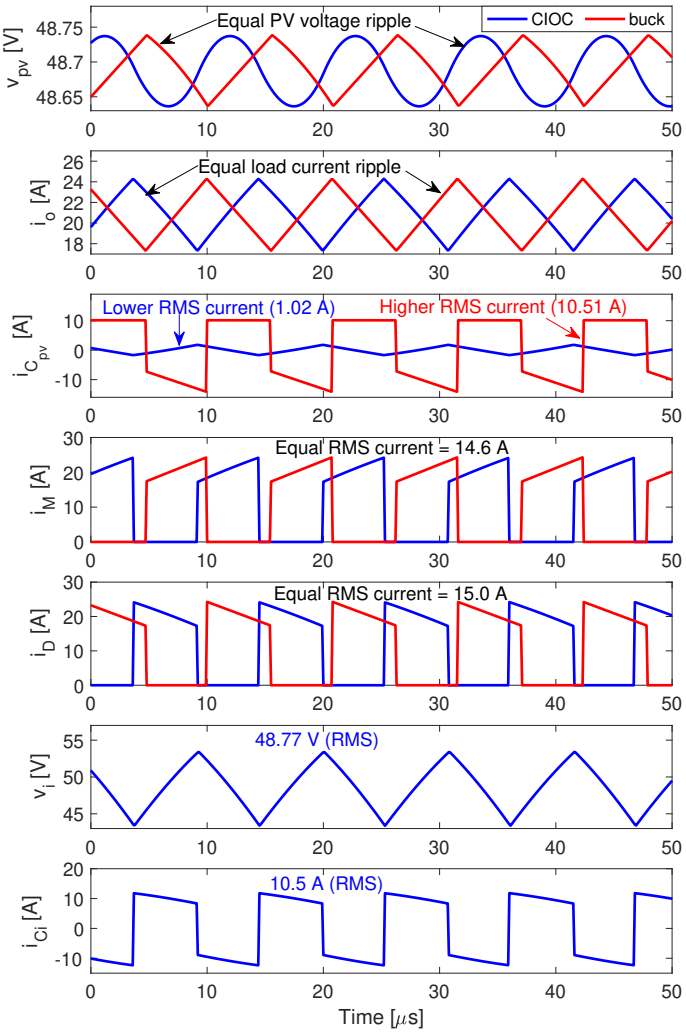

Figure 12. Performance comparison of PV systems based on both CIOC and classical buck converters.

Figure 12 also confirms the correct L_1, L_2, and C_{pv} design: the PV voltage ripple is 50.65 mV, which is lower than the design limit calculated in Section 6 ($\delta v_{pv} = 50.87$ mV).

Similarly, Figure 12 shows that the output current ripple is equal to 3.5 A, which is in agreement with the value predicted with Equation (50). In addition, the switching frequency in this steady-state condition is $F = 92.6$ kHz, thus fulfilling the design criterion imposed in Section 6 ($F \leq 100$ kHz). It must be noted that the switching frequency will never be higher than 100 kHz, hence the maximum switching losses can be estimated with such a limit frequency. In fact, the simulation reports that the switching frequency of both the CIOC and buck PV systems is the same, which is confirmed by the waveforms of the MOSFET and diode currents (i_M and i_D, respectively). Since both PV systems operate with the same switching frequency under steady-state conditions (92.6 kHz), the waveforms of the MOSFETs' and diodes' currents are the same, just displaced in time. This is further verified by calculating the RMS currents of the MOSFETs and diodes in both PV systems, obtaining the same value. Finally, taking into account that the MOSFET and diode waveforms are equal in both PV systems, the switching losses are thus also the same; for the example in Figure 12, these losses are, on average, 1.5 W per period considering a MOSFET on resistor equal to 4.8 mΩ, which corresponds to 0.3% of the generated power (500 W).

Figure 12 also shows the voltage and current on the intermediate capacitor C_i of the CIOC PV system, named v_i and i_{C_i}, respectively. Such a C_i capacitor was designed to ensure a small peak-to-peak ripple in v_i equal to 20% of the steady-state value, resulting in the small capacitor of 5.6 μF reported in Table 2. Therefore, the capacitive storage requirements of the CIOC are not significantly increased by C_i, since, in this example, $C_{pv} + C_i = 52.6$ μF, which is more than 10 times smaller than the capacitive requirement of the buck-based PV system. Figure 12 shows that the current in C_i is discontinuous, thus producing a large RMS current that must be supported by the capacitor; nevertheless, it is possible to find commercial film capacitors that support these RMS currents [59,60]. In case it is needed, increasing C_i to acquire a non-electrolytic capacitor with higher RMS current capability will reduce the v_i ripple, which will increase the power range in which the inductor currents are continuous, thus not affecting the system performance.

The second set of circuit simulations concerns the validation of the mathematical model proposed in Section 3, including the action of the SMC designed in Section 5. This validation is performed in both frequency and time domains. Figure 13 shows the frequency response of the closed-loop system generated by both the circuit simulation and the theoretical model previously reported in Equation (63). These results evidence the accurate representation provided by the mathematical model proposed in this paper, since both the amplitude and phase of the frequency response are correctly predicted. Moreover, such a Bode diagram also confirms the correct tracking of the reference v_r, where no error or phase shift is observed up to 1 kHz; thus, the step-like reference of the P&O will be tracked with null steady-state error.

In addition, the frequency response of the closed-loop circuit to perturbations in the load voltage is investigated in Figure 14. Such a Bode diagram confirms the correct mitigation of perturbations occurring in the load voltage, where the maximum perturbation transference is 0.62% (at 3.4 kHz). In fact, the perturbation transference at 120 Hz is 0.04%; thus, the voltage oscillations caused by the ac output of the inverter (load) will be satisfactorily rejected, and these oscillations will not interfere with the MPPT process.

The previous frequency-based results are complemented with the evaluation of the time-domain performance reported in Figure 15. Such a circuit simulation confirms the correct tracking of the reference provided by the SMC. Moreover, the circuital implementation of the SMC imposes the same dynamic performance predicted by the transfer function (63), thus confirming the correct implementation of both the power stage and control system. This circuit simulation also confirms the fulfillment of both the reachability and equivalent control conditions: First, the switching function Ψ is always trapped inside the hysteresis band ($-H$ to $+H$), thus the reachability conditions are fulfilled; therefore, the local stability is confirmed. Second, the duty cycle is always trapped inside the physical limits (0 and 1), hence no duty cycle saturation occurs. Both conditions confirm the global stability of the PV system.

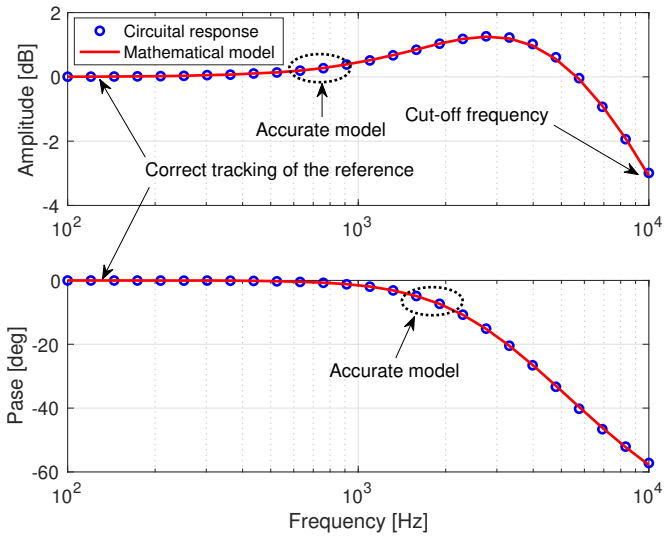

Figure 13. Frequency response of the PV system in closed loop.

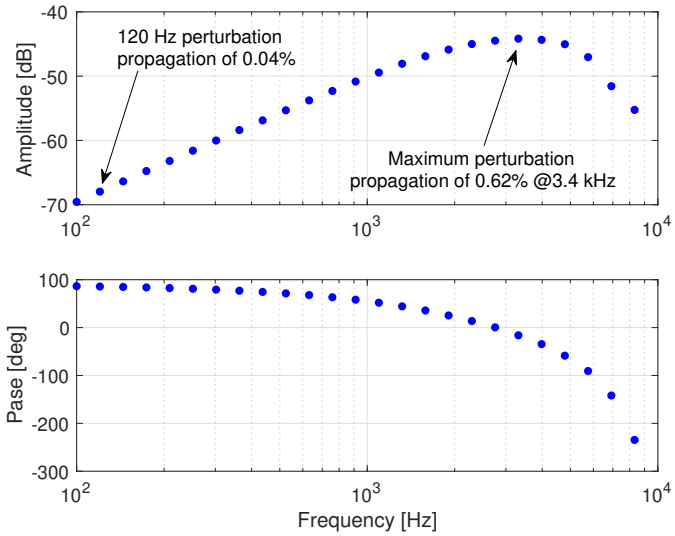

Figure 14. Perturbations mitigation in the closed-loop circuit.

The simulation results of Figure 15 also confirm that the switching frequency is always below the design limit (100 kHz), where high switching frequencies are imposed to provide fast tracking of the reference, returning to steady switching frequencies after the transient ends. Finally, these results also confirms the accurate settling time imposed by the SMC, which fits the design value (250 µs). Therefore, it is confirmed that the proposed PV system (power stage and SMC) fulfills the requirements to extract the maximum power from the PV source, even with load voltage perturbations.

An additional simulation was conducted to evaluate the controller performance under different perturbations at the load voltage. It is clear that 60 Hz inverters will produce perturbations at 120 Hz, and 50 Hz inverters will produce perturbations at 100 Hz; however, inverter failures or nonmodeled grid behaviors could produce additional perturbations to other frequencies. Therefore, the proposed PV system was tested under load voltage perturbations at multiple frequencies: 60 Hz, 120 Hz, 240 Hz, 500 Hz, 1 kHz, and 10 kHz. The results of such a test are presented in Figure 16, which confirm that the proposed SMC ensures the correct regulation of the PV voltage under different load voltage perturbations, thus not only the classical 120 Hz perturbation is compensated.

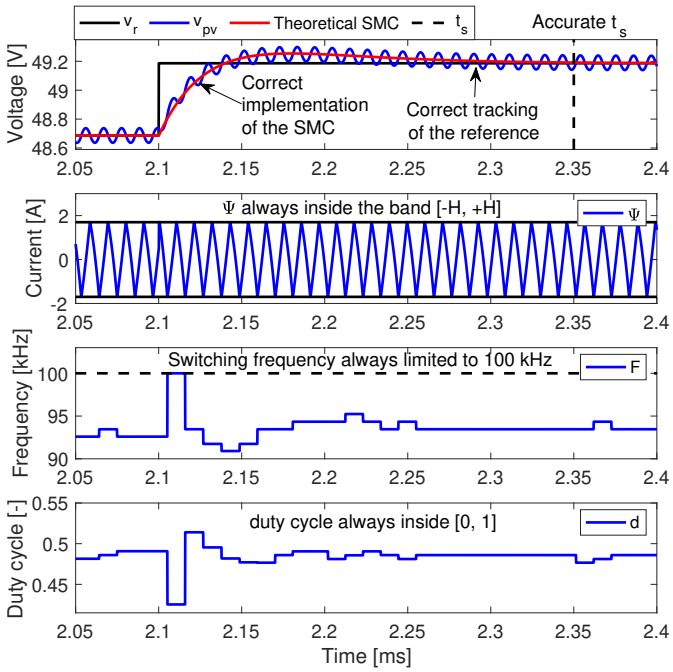

Figure 15. Performance of the PV system to changes on the reference value.

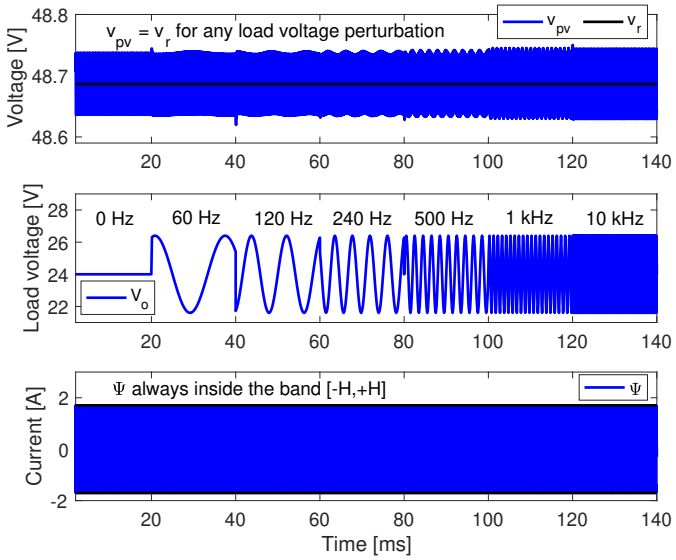

Figure 16. Performance of the PV system to different perturbations in the load voltage.

The previous conclusions are tested by implementing a circuit simulation of the complete PV system, including the P&O algorithm. Such simulation results are presented in both Figures 17 and 18. This final test considers a changing irradiance condition with fast transients of 1000 W/(m^2· s) (one sun per millisecond), starting a full irradiance (1000 W/m^2), then falling to a medium irradiance (600 W/m^2), and later falling to a low irradiance (200 W/m^2), recovering the full irradiance at the end of the profile. In addition, this test also considers a 20% voltage oscillation at 120 Hz perturbing the output of the CIOC converter, which emulates the connection with the commercial inverter COTEK SP-700-124 [8].

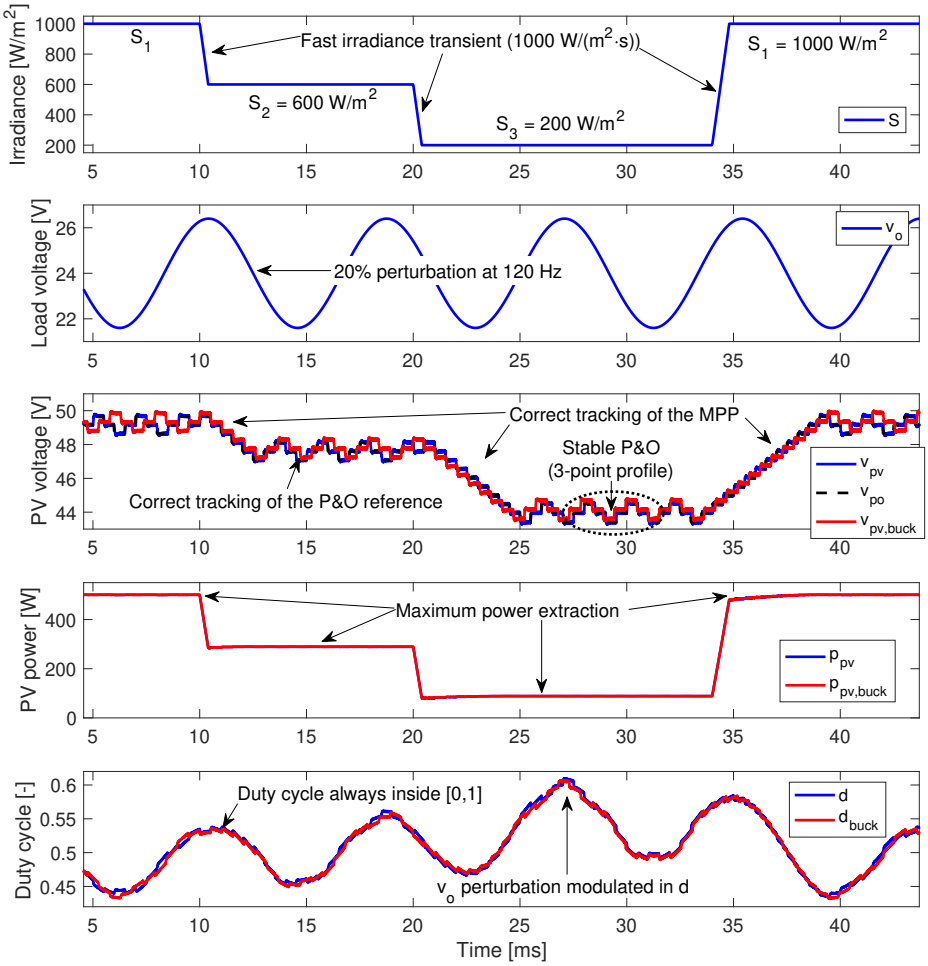

Figure 17. Maximum power point tracking using the CIOC converter with SMC and the classical buck converter with SMC.

The performance of the PV voltage confirms the correct tracking of the reference provided by the P&O, which is evident since both v_{pv} and v_{po} waveforms are superimposed. In addition, the PV voltage waveform also shows the three-point behavior typical of stable P&O algorithms operating at the optimal condition [46,49], which ensures that the P&O algorithm reaches the maximum power points (MPP). Moreover, the tracking of the new MPP is observed in each irradiance transition. The maximum power extraction and tracking are confirmed by the trajectories reported in Figure 18, which shows the paths taken to track each MPP. Finally, the successful operation of the PV system under load voltage oscillations is explained by the fact that these oscillations are modulated into the duty cycle, thus compensating them without saturating the duty cycle. Finally, Figure 17 also shows the dynamic simulation of the PV system based on the buck converter previously designed for comparison purposes (red waveforms). To provide a fair comparison, such a buck-based PV system was complemented with the same P&O algorithm [61] and with a sliding-mode controller designed as described in [28] to provide a similar settling time. The results confirm that both the proposed CIOC and buck-based solutions provide the same PV power, which is expected since the buck converter was designed to provide the same ripples as observed in Figure 12, thus resulting in the same duty cycle and similar voltage profiles but requiring much higher capacitive storage for the classical buck solution.

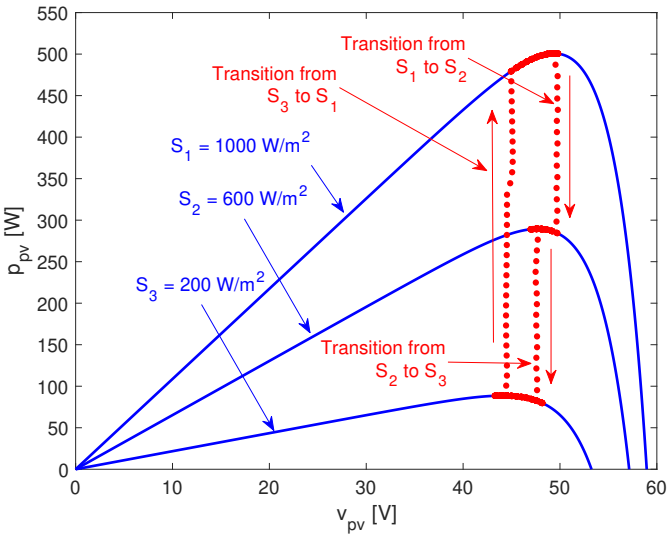

Figure 18. Maximum power point tracking trajectories.

In conclusion, the circuit simulations performed in this section confirm the following conditions:

- The CIOC converter was accurately designed to impose the desired current and voltage ripples to both the PV source and the load.
- The CIOC converter provides the same ripples in comparison with the buck converter, requiring the same inductive energy storage but with much lower capacitive energy storage, thus improving reliability.
- The SMC provides global stability to the PV system in any operating condition.
- The proposed PV system, based on the CIOC converter and SMC, ensures the extraction of the maximum power, even with high perturbations in the load voltage, which is a common case when inverters are added to the PV system to form a small-power microinverter.

8. Conclusions

A low-voltage photovoltaic system that uses a continuous input/output current buck converter was proposed in this paper. The design of the converter and its control systems included the definition of the maximum switching frequency of 100 kHz and the calculation of two inductances, $L_1 = L_2 = 38$ uH, two capacitances, $C_{pv} = 47$ uF and $C_i = 5.6$ µF, P&O algorithm parameters, $\Delta v_{po} = 500$ mV and $T_{po} = 500$ ms, three controller parameters $k_c = -1$, $k_p = 2.36$ A/V, and $k_i = 29.5$ kA/(V· s), and $H = 1.67$ A, which ensures the maximum switching frequency.

The main advantage of the proposed PV system is to impose desired current and voltage ripples to both the photovoltaic source and the load with lower input capacitance requirements than the classical buck converter. For instance, in a simulated application with the SP500M6-96 PV panel and the commercial inverter COTEK SP-700-124; the imposed PV voltage ripple was 50.87 mV, with an input capacitor of 47 µF and an internal capacitor of 5.6 µF. Moreover, the implemented P&O algorithm extracted the maximum power of the photovoltaic source, in this case 95 W, 297 W, and 500 W for three different irradiance values, and the proposed sliding-mode controller provided global stability to the system in any operating condition and rejected output perturbations, including the double-frequency oscillations of 120 Hz produced by an intended microinverter. To simulate the application example, circuit simulations, developed with the power electronics simulator PSIM, confirmed that the designed CIOC converter imposed the desired current and voltage ripple to both the PV source and the load. Moreover, the CIOC converter provided the same ripple

compared with the classical buck converter, requiring the same inductive energy storage but with lower capacitive energy storage.

Despite the advantages of the proposed low-voltage photovoltaic system, some requirements were faced to operate the system satisfactorily: a complex mathematical model of the converter to design the controllers, which also requires a complex theory to be analyzed and designed, and the design of the converter is more complex than the classical buck to achieve the requirements of the PV system.

For the implementation stage, two clear disadvantages will have to be covered: a greater number of elements than the classical buck converter, reducing the reliability of the system (one more inductor), and the design and implementation of the MOSFET driver in the high-voltage side of the system.

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Data Availability Statement: The data used in this study are reported in the paper figures and tables.

Conflicts of Interest: The authors declare no conflict of interest.

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